WHAT IS CLAIMED IS:

1. A method to recover a return path signal represented entirely as ones and zeros in a cable television system comprising the steps of:

receiving a serial stream of digital words with appropriate synchronization information to identify the boundaries between words and to recover timing of the bits themselves;

deserializing the serial stream of digital words and synchronization information;

processing the deserialized digital words to interface digitally to an application receiver; and

forwarding the processed parallel digital words to the application receiver.

2. A method according to Claim 1, wherein said processing step comprises the steps of:

eliminating front end analog stages of the digital words;

providing a digital word interface directly to a data bus to a digital receiver portion of a demodulator of the application receiver; and

replacing the functionality of the front end analog stages with equivalent digital functionality.

3. A method according to Claim 1, wherein said method is performed at a CATV headend.

4. A method according to Claim 1, wherein said method is performed at a CATV hub.

5. A method according to Claim 1, wherein the application receiver includes a digital demodulator with a digital receiver.

6. A method according to Claim 5, wherein if the digital receiver's data bus is smaller than the parallel word length, a digital filter truncates the least significant bits to interface to the application receiver.

7. A method according to Claim 5, wherein if a word size of the digital receiver exceeds that of the transmission link, the parallel word is padded with zeros.

8. A method according to Claim 1, wherein a logical translation device interfaces between an application receiver and the transport link.

9. A method according to Claim 8, wherein the logical translation device is part of the application receiver.

10. A method according to Claim 9, wherein the logical translation device is a Field Programmable Gate Array (FPGA).

11. A method according to Claim 10, wherein said FPGA processes the data words after the deserializing step deserializes the serial stream of digital words and synchronization information and formats the data for the application receiver's data bus.

12. A system for a recovering a return path signal of digital words, in a hybrid fiber-coax cable television system using baseband serial optical transport, in which the return path signal from the fiber optic node to the headend/hub is represented by encoding it entirely as ones and zeroes, the system including a digital return receiver and a plurality of application receivers, the digital return receiver of the system comprising:

conversion/receiving means for receiving a serial stream of optical ones and zeroes from an optical fiber and converting the optical digital signal to an electrical digital signal;

means for deserializing the serial stream of digital words and synchronization information;

digital processing means for processing the deserialized digital words to interface digitally to an application receiver; and

interface means for interfacing and forwarding the processed parallel digital words to at least one of the plurality of application receivers.

13. A system according to Claim 12, wherein said digital processing means comprises:

means for eliminating front end analog stages of the digital words;

means for providing a digital word interface directly to a data bus to a digital receiver portion of a demodulator of the application receiver; and

means for replacing the functionality of the front end analog stages with equivalent digital functionality.

14. A system according to Claim 12, wherein said system is implemented at a CATV headend.

15. A method according to Claim 12, wherein said system is implemented at a CATV hub.

16. A system according to Claim 12, wherein the at least one application receiver includes a digital demodulator with a digital receiver.

17. A system according to Claim 16, wherein if the digital receiver's data bus is smaller than the parallel word length, a digital filter of said digital processing means truncates the least significant bits to interface to the at least one application receiver.

18. A system according to Claim 16, wherein if a word size of the digital receiver exceeds that of the transmission link, the parallel word is padded with zeros.

19. A system according to Claim 12, wherein a logical translation device interfaces between the at least one application receiver and the transport link.

20. A system according to Claim 19, wherein the logical translation device is part of the application receiver.

21. A system according to Claim 20, wherein the logical translation device is a Field Programmable Gate Array (FPGA).

22. A system according to Claim 21, wherein said FPGA processes the data words after said deserializing means deserializes the serial stream of digital words and synchronization information and formats the data for the application receiver's data bus.